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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,583	12/21/2000	Daniel Leibholz	SMQ-023	3889

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,583	LEIBHOLZ ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims1-2 and 8-19 rejected under 35 U.S.C. 102(e) as being anticipated by Lin U.S. Patent Number 6,631,452 (herein referred to as Lin).

2. Referring to claims 1 and 14 Lin has taught. A microprocessor, comprising:

registers for holding values, wherein said registers are logically partitioned into register windows (Lin figure 2, figure 4, column 4 lines 1-29; the frames are the register windows);

a storage for storing values held in the registers of the register windows (Lin figure 2, figure 4, column 4 lines 1-29; the backing store);

a detector for detecting that one of a register window overflow condition and a register window underflow condition is imminent (Lin column 8 line 49-column 9 line 5, figure 6; the mandatory fill and spill operations come from underflow and overflow conditions); and

an instruction generator responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap responsive to the condition that is detected as imminent (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract).

3. Referring to claims 2 and 15 Lin has taught wherein the detector and the instruction generator are implemented in hardware (Lin column 11 lines 1-15).

4. Referring to claim 8 Lin has taught wherein the detector detects solely whether a register window underflow condition is imminent (Lin column 11 lines 40-43).

5. Referring to claim 9 Lin has taught wherein the detector detects solely whether a register window overflow condition is imminent (Lin column 11 lines 35-39).

6. Referring to claim 10 Lin has taught wherein the detector detects both whether a register window overflow condition is imminent and whether a register window underflow condition is imminent (Lin column 8 line 49-column 9 line 5, figure 6; the mandatory fill and spill operations come from underflow and overflow conditions).

7. Referring to claim 11 Lin has taught wherein the microprocessor further comprises an execution unit for executing the instruction generated by the instruction generator (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 4).

8. Referring to claim 12 Lin has taught wherein the microprocessor performs out of order execution of instructions (Lin column 3 lines 32-45; speculative processing by definition is not a certain operation, but is a prediction based on some information, and because of a misprediction, the wrong order of operations will occur).

9. Referring to claim 13 Lin has taught wherein the instruction generator includes a second storage for holding the at least one instruction that is generated by the instruction generator (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract; it is inherent that some ROM or other memory would be available to hold the speculative operations, that the RSE chooses to executes).

10. Referring to claim 16 Lin has taught a microprocessor having a plurality of registers logically partitioned into register windows and a storage for storing contents of register windows, a method, comprising the steps of:

determining that one of a register window overflow condition and a register window underflow condition is imminent (Lin column 8 line 49-column 9 line 5, figure 6, column 5 line 46-column 6 line 2, abstract; the mandatory fill and spill operations come from underflow and overflow conditions); and

in response to determining that the one of the register overflow condition and register window underflow condition is imminent, manipulating the storage to avoid a trap responsive to the condition determined as imminent (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract).

11. Referring to claim 17 Lin has taught wherein, when it determined that a register window overflow condition is imminent, the step of manipulating the storage comprises providing at least one instruction for execution by the microprocessor that causes the contents in at least the selected register window to be stored in the storage (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract).

12. Referring to claim 18 Lin wherein, when it is determined that a register window underflow condition is imminent, the step of manipulating the storage comprises providing at least one instruction for execution by the microprocessor that causes data in the storage to be stored in the registers (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract).

13. Referring to claim 19 Lin has taught wherein the microprocessor has an instruction stream slated for execution and wherein the instruction that causes the contents in at least the selected register window to be stored in the storage is inserted into the instruction stream (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 4; the instruction stream is the operations in figure 4 that spill and fill the registers from memory).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin.

15. Referring to claim 3 Lin has not taught wherein the microprocessor further comprises a cache for caching instructions for introduction into an execution stage and wherein the detector examines the instructions in the cache to determine if a register window overflow condition is imminent by determining if execution of any of the fetched instructions will result in a register window overflow condition. However Lin has taught that it is desirable to monitor instructions to be able to see if one of those instructions will cause a mandatory stall, and if an instruction is found that does, to speculatively fill and spill the registers in the stack to save or restore the registers to prevent the stall from happening (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 6). One of ordinary skill in the art at the time of the invention looking at Lin would recognize that Lin is teaching to look ahead to see what is going

to happen with the instructions. Therefore, one of ordinary skill in the art at the time of the invention looking at Lin would recognize the advantage of looking further up the instruction path into the instruction cache to see what instructions are coming up, to give the system even more time to save or restore registers to prevent exceptions and stalls and traps, which consume time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to look in the instruction cache for instructions that would cause a stall to prevent the stall from happening to reduce the time needed for execution.

16. Referring to claim 4 Lin has taught wherein the detector looks for an instruction in the cache that stores contents of a register window in the registers when the registers have no available space for storing the contents (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 6, column 8 line 49-column 9 line 5).

17. Referring to claim 5 Lin has taught wherein the detector examines how much storage space is available in the registers (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 6, column 8 line 49-column 9 line 5).

18. Referring to claim 6 Lin has not taught wherein the microprocessor further comprises a cache for caching instructions for introduction into an execution stage and wherein the detector examines the instructions in the cache to determine if a register window underflow condition is imminent by determining if execution of the instructions will result in a register window underflow condition. However Lin has taught that it is desirable to monitor instructions to be able to see if one of those instructions will cause a mandatory stall, and if an instruction is found that does, to speculatively fill and spill the registers in the stack to save or restore the registers to prevent the stall from happening (Lin column 7 line 45-column 8 line 15, column 5 line 46-

column 6 line 2, abstract, figure 6). One of ordinary skill in the art at the time of the invention looking at Lin would recognize that Lin is teaching to look ahead to see what is going to happen with the instructions. Therefore, one of ordinary skill in the art at the time of the invention looking at Lin would recognize the advantage of looking further up the instruction path into the instruction cache to see what instructions are coming up, to give the system even more time to save or restore registers to prevent exceptions and stalls and traps, which consume time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to look in the instruction cache for instructions that would cause a stall to prevent the stall from happening to reduce the time needed for execution.

19. Referring to claim 7 Lin has taught wherein the detector looks for an instruction in the cache that restores a register window when contents of the register window are stored on the stack rather than in the registers (Lin column 7 line 45-column 8 line 15, column 5 line 46-column 6 line 2, abstract, figure 6, column 8 line 49-column 9 line 5).

Response to Arguments

20. Applicant's arguments filed 11/09/04 have been fully considered but they are not persuasive.

21. In the remarks, in regard to the rejection of the claims, Applicant argues in essence that:

> "Lin does not disclose a mechanism for generating an instruction to avoid a trap from a register window overflow or underflow condition in response to detecting the register window overflow or underflow condition."

22. This is not found persuasive. Lin detects an overflow or underflow condition in the same manner as described in the claims. Then Lin issues operations to take care of spilling or filling the registers from memory to avoid a situation where the data is "spilled" over the register stack. If Lin didn't spill enough registers when an overflow condition is imminent, then the data would spill over the top of the stack, and overwrite registers that have not been saved. Lin's system prevents this scenario from occurring, and thus saves time. In addition, Lin also teaches speculative fill and spill of the registers when bandwidth is available to help reduce stalls.

Nowhere in the claims does Applicant claim where his invention "avoids stalls", yet Applicant argues the point in his response. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., avoids stalls) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Also, Examiner wishes to point out that in claim 3, Applicant does not say when the instructions in the cache are examined. Therefore, the instructions in the cache could be examined when they make their way into the pipeline and the execution units.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167. The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Patent Examiner

Art Unit 2183

December 6, 2004

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